TI 35E
image reversal resist

Technical Data Sheet
revised 08/2016

MicroChemicals GmbH
Nicolaus-Otto-Str. 39
D-89079 Ulm
Fon +49 (0) 731 977343 0
Mobil +49 (0) 177 3332453
Fax +49 (0) 731 977343 29
Email info@microchemicals.com
Internet www.microchemicals.com

General Information

The TI 35E resist is specially designed for the application in the so called "image reversal technology" for:

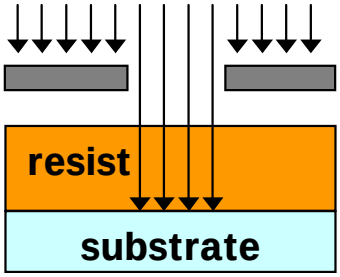
- **subsequent lift-off of deposited layers**
- **wet chemical treatment in HF containing etching solutions**
- **direct mesa grooving.**

The viscosity of the resist leads to a thickness range depending on the spin-speed from 3.0-4.5 µm. With spin-speed of 3000 rpm a resist thickness of 3.6 µm will be achieved that enables lift-off of evaporated solids up to a thickness of 6 µm. The typical aspect ratio of the structured features achievable is in the range of 1.6 .. 2.0.

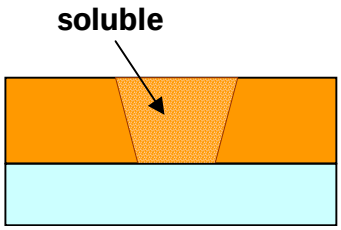
This technical data sheet intends to give you a guide-line for process parameters for various applications. However, the optimum values for e.g. spin profile, exposure dose, or development depend on the individual equipment and need to be adjusted on each individual demand.

'Image Reversal' – A Short Introduction

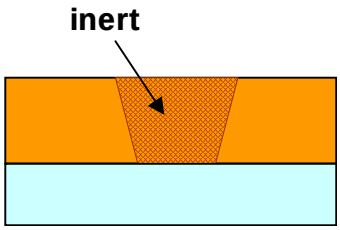
What 'image reversal' generally means



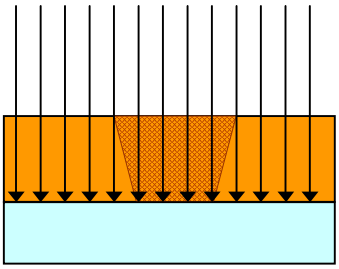
(1) Exposure using an inverted mask (the exposed areas finally remain)



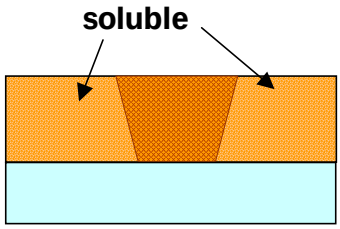
(2) The resist now would behaves like an exposed positive resist.



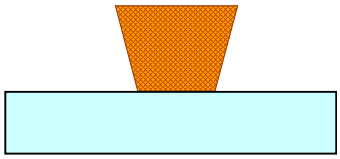
(3) The reversal bake cross-links the exposed area, while the unexposed area remains photo-active



(4) The flood exposure (without mask) ...



... (5) makes the resists, which was not exposed in the first step, soluble in developer



(6) After developing, the areas exposed in the first step now remain

... and for what image reversal is good for:

® **High stability for wet-chemical etching allows the usage of the inverted TI 35E as mask for wet-chemical etching under harsh conditions**

TI 35E – Fields of Application

Lift-off of PECVD layers

- Amorphous Si layer deposited in device quality at 110°C
- Amorphous SiN_x

Lift-off of sputtered layers

- Due to non-directional deposition, lower thickness achievable (approx. 1 µm)
- Possibly ultra sonic treatment necessary
- Liftability dependent on operating pressure

Etching of SiN_x in BHF (12.5 % HF)

- SiN_x deposited at 400 °C with PECVD
- Hardbake at 125°C (Hotplate) for two minutes
- No visible degradation of resist after 10 min etching time
- Enables structuring of SiN up to at least 100 nm (tested)
- Use ammonia during SiN_X deposition to increase adhesion of the resist on the surface
  (For harsh chemical attack prefer the use of TI 35E)

Etching of thick thermal SiO_2 with 20 % HF

- No visible degradation of the resist after 10 min
- Possible etching in HF conc. (50%) for several minutes
  (For harsh chemical attack prefer the use of TI 35E)

Direct mesa grooving

- TI series resists allow direct Si etching without SiO_2 masking
- Hardbake at 120-145°C for 2 min necessary
- Use HNO_3 (70%) : HF (50 %) : H_2O = 75 : 10 : 25 as etching solution and TI 35E resist in reversal mode, groove up to 4 µm in 45s

Technological Requirements

Since the TI 35E yields an inverted structure in the image reversal mode, an inverted exposure mask is needed. Beyond this, compared to standard positive resist processing, no further upgrade in existing technological infrastructure is necessary.

Also compared to standard positive resist processing, applying the TI 35E implements just two further process steps: The reversal bake and the flood exposure without mask, both very easy to be performed and explained in the following.

Processing the TI 35E

(in chronological order)

- **Substrate preparation: Put the substrate on the hotplate at a minimum temperature of 120 °C for 10 minutes to remove adsorbed water from the substrates surface. Alternatively, you can use a furnace at same temperature for 30 min. Of course standard HMDS procedure (only from vapor phase at an optimum substrate temperature of 125°C!) is also an adequate preparation.**

- **Spin-coat the resist after cooling down the substrates, spin at the final speed level for at least 30-40 seconds.**

- **Softbake the coated substrate at 95°C for 2 minutes on the hotplate (when using a furnace, 95°C for 20 min is recommended)**

- **Exposure the coated substrate (with the mask) at a dose of 140 mJ/cm^2. This first exposure dose adjusts the negative wall profile the so called "undercut". Lower the 1st exposure dose to increase the undercut. 140 mJ/cm² will be a good choice for most applications. A too low 1st exposure dose will dramatically increase the erosion of the resist not to be cleared (see appendix). Note: Exposure dose holds for calibration on i-line (365nm). A standard mask aligner with a 350W Hg lamp has approx. 10 mW/cm^2 i-line intensity.**

- **Keep the coated substrate at room temperature after the exposure for at least 10 minutes. In this delay time nitrogen, generated during exposure, will diffuse out the resist. If you use square shaped substrates the resist thickness on the edges is significant thicker than 3-4 µm. In this case the nitrogen needs more time to diffuse out. In this case double the delay time.**

- **After the delay bake the coated substrate on the hotplate at a temperature of 115 .. 120°C on the hotplate for two minutes (when using furnace try 20 minutes at 115°C. Because this step is very temperature critical furnace baking is not recommended). This step is the *reversal bake* where the image is reversed due to cross link the exposed areas making them insoluble in the developer.**

- **Exposure the coated substrate for the second time without a mask (flood exposure). Use a dose (very uncritical) of 540 mJ/cm^2 (200-800 has not a dominant effect). When, during a subsequent deposition, the temperature will raise over 80°C use high exposure doses to avoid nitrogen bubbles in the resist during the deposition. Especially when UV-light is present during deposition (plasma coating).**

- **Develop in AZ developer such as 826MIF (metal ion free) or potassium or sodium based developer (AZ 400K 1:4). When the structure is through-developed (cleared), add another 10-30% in the bath of the total development time to finalize the side wall profile.**

- **Hardbake the coated substrate only when using the resist as an etching mask under harsh conditions. When using it for mesa grooving hardbake at 140°C to 145°C for 2 minutes on the hotplate. The side-wall profile will loose the undercut during this step, lift-off processes become more problematic. If you need a hardbake and lift-off or very high temperatures during deposition, make a UV-curing to harden the resist after development (or contact us for further information).**

Processing the TI 35E - Overview

Resist thickness (µm)	3.0... 4.5
Exposure Broadband or g, h, i (mJ/cm^{-2})	100 .. 250, 140 (typ.)
Typical Exposure time (sec)*	10-25, 14 (typ.)
Reversal Bake Time (Hot plate Temperature)	2 min (115-120°C)
Flood exposure (mJ/cm^{-2}) (without any mask)	540 (typ.) 200-800
Developer	Clariant AZ 351B, MIF Developers e.g. AZ 826
Hardbake 140 ... 145°C (only for hard etching, avoid it for lift-off)	2 min
Lift off media	PGMEA, NMP, MMP, EEP, DMF, Acetone, ethyl lactate
Remover (Stripper)	AZ 100 remover, acetone

*Exposure dose as calibrated on i-line (365nm). A standard mask aligner with a 350W Hg lamp has approx. 10 mW/cm^2 i-line intensity